An ECG measurement IC using driven-right-leg circuit

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***Abstract*— In this paper, an electrocardiographic (ECG) signal processing IC, which will be used for portable biomedical application, was designed using continuous-time technique. The circuit consists of an instrumentation amplifier (INA) with driven-right-leg circuit (DRL), a 5th order G_m-C low pass filter (G_m-C LPF) operating in sub-threshold mode, and amplifiers. DRL circuit is used to detect small amplitude signal in the presence of large common-mode voltage from the human body. The CMRR of the INA is 78 dB and the G_m-C LPF has a cutoff frequency of 18 Hz. As a result of using the DRL, a small signal can be detected in the presence of large common-mode differential. The circuit consumes 1.23 mW when operating from with a supply voltage of ±1.5-V and occupies a core area of 0.94 mm^2. The circuit was designed in a 0.35μm CMOS process and simulation results have successfully demonstrated the functionalities.**

I. INTRODUCTION

The purpose of this work was to develop an ECG signal acquisition circuit that will be a part of the portable multi-function system for the monitoring of biomedical signal and measurement of vital sign such as blood pressure and heart rate.

Traditionally, ECG signal is measured using three electrodes, as shown in Fig. 1. High CMRR (greater than 80 dB) is required in order to amplify small differential signals in the presence of large common mode voltages [1]. This setup, however, might not be suitable for the detection of small differential voltages (in the order of 10 to 100 μV) with large common-mode differential, which is the case in human body. In addition, most of the designs of ECG signal processing circuit in literature involve switched-capacitor (SC), chopper technique or the usage of large external components in the design of its INA and filters [2]-[8]. For the processing of biomedical signal, continuous time technique (G_m-C) is preferable to discrete time technique (SC) and modulation technique (chopper). To illustrate the point, if a very low cutoff frequency filter is implemented using SC, the hold time would be very long and that would induce some leakage current inevitably. Also, complex clock circuitry is required to operate SC circuit. Though chopper technique can remove the 1/f noise of the system, it introduces residual offsets caused by spikes [4]. Therefore, some other means of implementation is worthy of investigation.

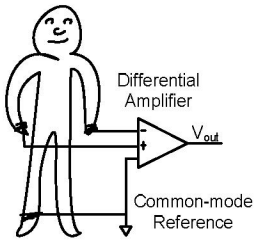

Fig. 1. Typical measurement of biopotentials.

This paper proposes some simple techniques to address the design of a robust analog front-end that rejects large input differential effectively, and to address the implementation of a continuous-time signal processing system. In section II, the sensor architecture is explained. The building block circuits and simulation results are presented in section III and IV, respectively.

II. SENSOR ARCHITECTURE

The block diagram of the system is illustrated in Fig. 2, which consists of the three electrodes, instrumentation amplifier (INA), 5th order G_m-C low-pass filter (G_m-C LPF), and amplifiers. The focus of this work is enclosed within the box. The signal is acquired through the two electrodes in the presence of large input differential, where the third electrode is connected to the driven-right-leg (DRL) circuit to further reduce the common-mode voltage, the operation of which will be explained later. After this differential ECG signal is amplified, it passes through an off-chip DC blocking circuit and is then low-pass filtered and amplified to the desired level. There are various gain settings to accommodate a range of different input signals.

With regard to the rejection of large input differential voltages in section I, various techniques have been developed to overcome this problem [2]-[6]. Current conveyor (CC) and SC techniques are very popular in the implementation of INA; however, they are not effective in rejecting large input differentials.

Alternatively, there is another technique that has not been explored in silicon, but it has been used widely in discrete

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component technique, which is the driven-right-leg (DRL) system [9]. It works by sensing the common-mode voltage on the body and fed back to the right leg. This negative feedback drives the common-mode voltage to a low value. In this paper, DRL is incorporated in the design of the INA.

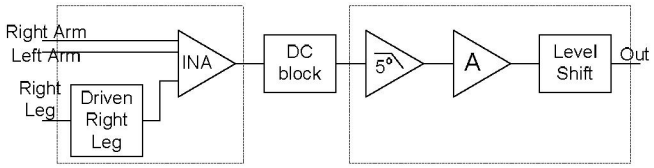

Fig. 2. Block diagram of the ECG measurement circuit

III. Building Block Circuits

A. *Instrumentation amplifier with driven-right-leg system*

The INA circuit (Fig. 3) has a gain of 8 V/V. The amplifier is taken from the two-stage amplifier in [10]. The circuit is similar to the one reported in [11]. It employs CC technique to circumvent the need of resistor matching in order to achieve a good CMRR. The differential signal (v_d) applies across v_1 and v_2 of Fig. 3 induces a current i_x to flow through $R_{1a,b}$. Then i_x is mirrored to R_2 very accurately through the two current mirrors. The first mirror senses the current entering the positive power terminal of one opamp. The second mirror senses the current exiting the opamp through the negative power terminal. Then this current will be summed via the virtual ground and converted to an output voltage through a transconductance amplifier. The CMRR can be approximated by the following:

$$CMRR = \frac{A_D}{A_{CM}} = \frac{A_{OL1}A_{OL2}}{A_{OL1} - A_{OL2}} \quad (2)$$

where $A_{OL1,2}$ is the open-loop gain of A_1 and A_2, respectively.

In order to further reject the common-mode of the human body, the reference node (V_{DRL}) is connected to the driven-right-leg (DRL) system. DRL has been used widely in the design of discrete ECG system for many years [9], but it has never been realized on chip. It works by sensing the common-mode voltage on the body by the averaging resistors R_i, inverted, amplified, and fed back to the right leg. This negative feedback drives the common-mode voltage to a low value. This is illustrated in Fig. 4 and the reduction of V_{cm} can be achieved by increasing the gain of amplifier, as seen from the following equation:

$$V_{cm} = \frac{R_{RL} i_d}{1 + 2R_f / R_i} \quad (3)$$

The body's displacement current (i_d) does not flow to ground but flows to the opamp output. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

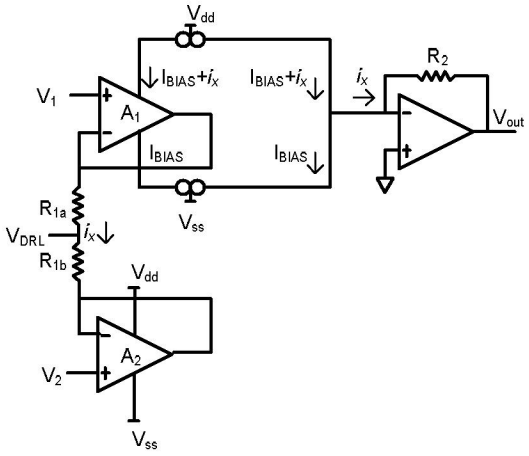

Fig. 3. Schematic of INA.

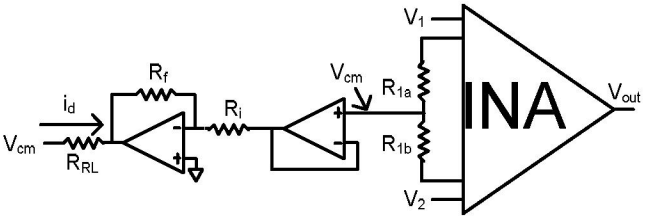

Fig. 4. Driven-Right-Leg circuit

B. *G_m-C Low-pass filter*

The G_m transconductor is shown in Fig. 5. It is implemented using sub-threshold and current reduction technique [12]. In this application, the transistor biased in triode region, MR, is split into two transistors and its source-gate voltage is controlled by MC1. The transconductances of the OTA can be tuned by VB2 and VB3. VB2 and VB3 provide flexibility in testing, and will be combined in later version. Transistors MM, M1 and MN are operating as source followers. The differential input voltage (v_1-v_2) is converted to current through transistor MR. The drain current of MR is split by transistors MM, M1 and MN. Most of the current flows to ground through transistors MM because the $g_{mMM} >> g_{mM1}, g_{mMN}$. Current reduction is achieved by the partial cancellation of drain currents of M1 and MN at the output. The small signal transconductance is

$$G_m = \frac{i_o}{v_1 - v_2} = \frac{N-1}{M+N+1} g_{oMR} \quad (4)$$

where g_{oMR} is the small signal drain-source conductance of transistor MR, given by

$$g_{oMR} = \mu_P C_{ox} \frac{W_{MR}}{L_{MR}} (V_{SGMR} - V_T) \quad (5)$$

In the above equations, M is the ratio of transconductances between MM and M1, while N is the ratio of transconductances between MN and M1. V_{sgmr} is the source-gate voltage of MR. Small G_m can be obtained by adjusting

the M and N ratios and reducing g_{oMR}. Transistors MM, M1, and MN are biased near the weak inversion region.

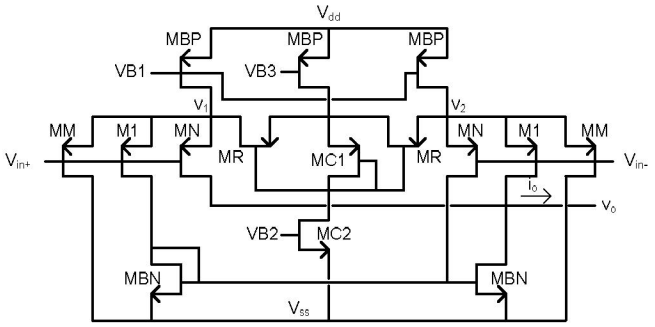

Fig. 5. Schematic of OTA

Three of the OTAs are used to implement a 2nd order LPF. A 5th order LPF is implemented by cascading multiple filters. The architecture is shown in Fig. 6. It has a cutoff frequency of 18 Hz and capacitors ranging from 8 pF to 0.01 pF were used. The disparate sizes of capacitor are not an issue here since matching is not important.

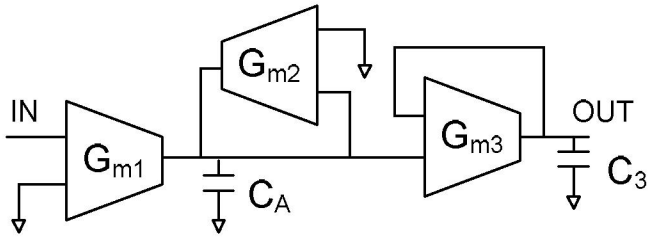

Fig. 6. 2nd order Gm-C LPF

C. *Amplifiers*

Resistive feedback amplifiers employing a two-stage opamp are used to amplify the filtered signal.

IV. POST-LAYOUT SIMULATION RESULT

A. *Instrumentation amplifier and driven-right-leg circuit*

The nominal and worst case simulations of CMRR is shown in Fig. 7. The INA achieved a CMRR of 78 dB. It can be seen that the circuit is robust in rejecting common-mode in the presence of process and temperature variations.

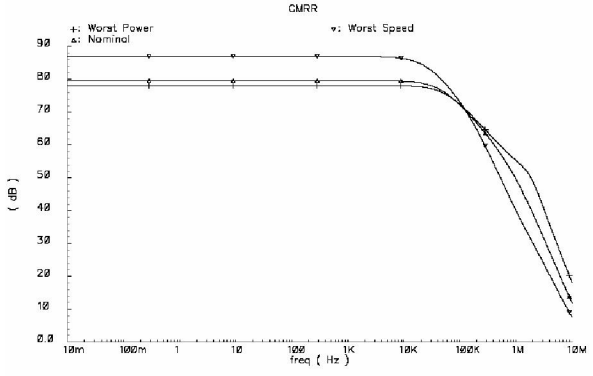

Fig. 7. Worst case and nominal simulation of CMRR of INA.

In order to demonstrate the functionality of the DRL circuit, the setup shown in Fig. 8 is simulated for the effects of DRL in response to input differentials. The transient responses of the circuit with and without the DRL are shown in Fig. 9. According to (3), V_{cm} dropped when the gain of the feedback amplifier increases. It can be seen that the differences in output amplitude is 60 µV without DRL and this could have a significant impact on the circuit when the input signal level is in the range of 100 µV to 500 µV.

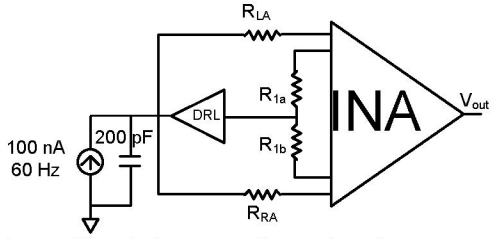

Fig. 8. Simulation setup for testing the DRL.

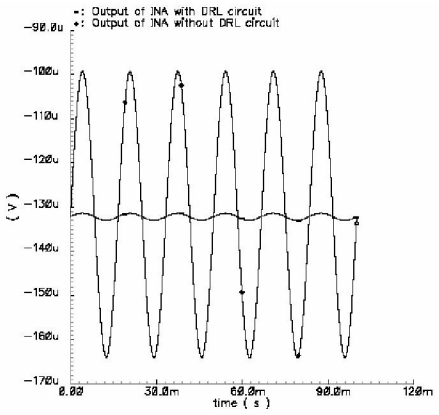

Fig. 9. Effect of output voltage with DRL and without DRL.

B. *G_m-C low-pass filter*

Fig. 10 demonstrates the immunity of the frequency response of the G_m-C LPF under different process temperature variations by tuning VB1, VB2 and VB3. It can be seen that the cutoff frequency is around 18 Hz.

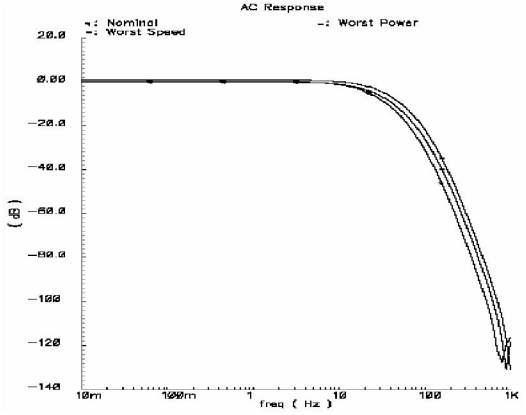

Fig. 10. Frequency response of Gm-C LPF in the presence of temperature and process variation

The simulated harmonic distortion components for a 100 mV/18 Hz input signal are shown in Fig. 11. It can be seen that HD3 is -43.1 dB.

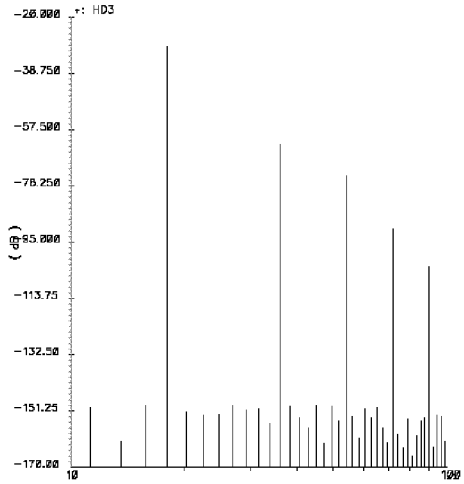

Fig. 11. Simulated harmonic distortion components for the filter.

C. *Additional results*

The overall transient simulation is shown in Fig. 12 and the layout of the chip is shown in Fig. 13.

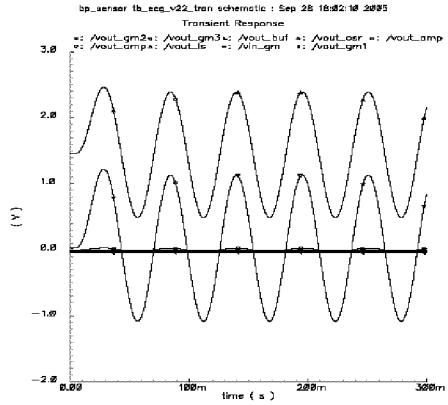

Fig. 12. Overall transient simulation of the circuit.

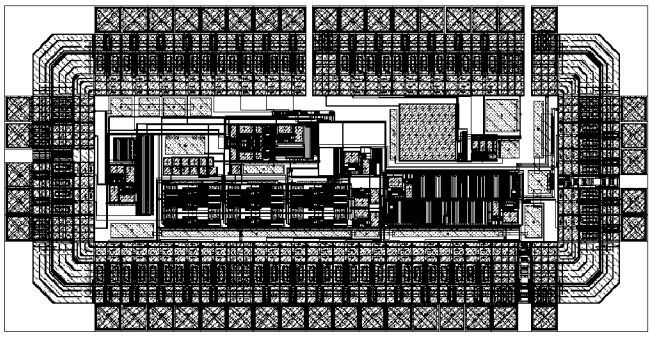

Fig. 13. Layout of the ECG IC.

V. Conclusion

The implementation of a continuous-time ECG signal processing circuit with robust common-mode rejection ability is presented. Simulation result shows that the DRL circuit can effectively reject the common-mode differential, have verified the CMRR of the INA, and different parts of the system in the presence of process and temperature variation as well as its functionalities.

Acknowledgment

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